Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALTUG KOKER and RUSSELL W. DYER

Appeal No. 2004-0524
Application No. 09/372,296

ON BRIEF

Before JERRY SMITH, LEVY and NAPPI, **Administrative Patent Judges**.

NAPPI, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 of the final rejection of claims 1 through 21, which constitute all the claims in the application.

Invention

The invention relates to a method for reducing bus access latency by prefetching data from memory (see page 5 of appellants' specification). The data is cached in a cache queue and then when the data is requested, it is transferred from the cache queue to a bus (see page 8 of appellants' specification).

Claim 1 is representative of the invention and reproduced below:

1. A method comprising:
pre-fetching a plurality of data from a memory to a data queue in response to a request; and
delivering the pre-fetched data from the data queue to a bus independently of the memory.

References

The references relied upon by the examiner are:

Kasper	6,356,962	March 12, 2002 (filed September 30, 1998)
Greiner et al. (Greiner)	6,216,208	April 10, 2001 (filed December 29, 1997)

Rejections at Issue

Claims 1, 4, 5, 8 and 15 stand rejected under 35 U.S.C. § 102 as being anticipated by Greiner. Claims 2, 3, 9 through 12 and 16-19 stand rejected under 35 U.S.C. § 103 as being obvious over Greiner and Kasper. Claims 6, 7 13,14, 20 and 21 stand rejected under 35 U.S.C. § 103 as being obvious over Greiner and official notice. Throughout the opinion we make reference to the brief[1] and the answer for the respective details thereof.

Opinion

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of anticipation and obviousness relied upon by the examiner as support for these rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants'

[1] Appellants filed an Appeal Brief on April 28, 2003.

arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

With full consideration being given to the subject matter on appeal, the examiner's rejection, the arguments of appellants and the examiner, and for the reasons stated *infra* we will not sustain the examiner's rejection of claims 1, 4, 5, 8 and 15 under 35 U.S.C. § 102, nor will we sustain the examiner's rejection of claims 2, 3, 6, 7, 9 through 14, and 16 through 21 under 35 U.S.C. § 103.

Appellants argue, on page 7 of the brief, that:

> Greiner does not disclose, either expressly or inherently, a prefetcher to prefetch data from a memory to a data queue and a queue controller to deliver the perfeched [sic] data from the data queue to a bus independently of the memory. As clearly shown in figure 2 in Greiner, the prefetch queue receives the address information from the internal queue, not from a memory. Furthermore, the element 162 is an address buffer to store addresses associated with the request, not the data.

The examiner's rejection of claims 1, 4, 5, 8 and 15 under 35 U.S.C. § 102 is set forth on pages 3 through 5 of the examiner's answer dated July 11, 2003. On page 4 of the answer, the examiner equates Greiner's element 120 of figure 1 with the claimed data queue.

Before we consider the teachings of Greiner we must first determine the scope of the claim. Claims will be given their broadest reasonable interpretation consistent with the specification, limitations appearing in the specification will not

be read into the claims. ***In re Etter*** 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985). In analyzing the scope of the claim, office personnel must rely on the appellant's disclosure to properly determine the meaning of the terms used in the claims. ***Markman v. Westview Instruments, Inc.***, 52 F3d 967, 980, 34 USPQ2d 1321, 1330 (Fed. Cir. 1995). "[I]nterpreting what is *meant* by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.'" (emphasis original) ***In re Cruciferous Sprout Litigation,*** 301 F.3d 1343, 1348, 64 USPQ2d 1202, 1205, (Fed. Cir. 2002) (citing ***Intervet America Inc v. Kee-Vet Laboratories Inc.*** 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)). "[T]he terms used in the claims bear a "heavy presumption" that they mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art." ***Texas Digital Sys, Inc. v. Telegenix, Inc.,*** 308 F.3d 1193, 1202, 64 USPQ2d 1812, 1817 (Fed. Cir. 2002).

Independent claim 1 includes the limitation "pre-fetching a plurality of data from a memory to a data queue" and "delivering the data from the data queue to a bus." Independent claims 8 and 15 contain similar limitations. The common meaning in the computer arts for the term "queue" is:

> A multi-element data structure from which (by a strict definition) elements can be removed only in the same order in which they were inserted; that is, it follows a first in, first out (FIFO) constraint. There are also several

> types of queues in which removal is based on factors other than order of insertion- for example, some priority value assigned to each element [2]

Thus, we interpret the limitation of a data queue to be a data structure in which removal of data is based upon some priority value.

We do not concur with the examiner's rationale that the cache, element 120, in Greiner, is the equivalent to the claimed queue. We find that Greiner teaches that when data is pre-fetched it is stored in a cache (see Column 3, lines 4-19). Greiner teaches that the cache is an internal memory (see column 2, lines 27 through 34) and that the data is removed from the cache based upon the memory address of the information requested (see column 5, lines 54-56). However, we find no teaching in Greiner that the cache operates such that data is removed based upon some priority value. Thus, we find that Greiner does not teach all of the limitations of independent claims 1, 8 and 15. Accordingly we will not sustain the examiner's rejection of claims 1, 4, 5, 8 and 15 under 35 U.S.C. § 102.

We next consider the examiner's rejection of claims 2, 3, 9 through 12 and 16-19 under 35 U.S.C. § 103 as being obvious over Greiner and Kasper. The examiner's rejection of claims 2, 3, 9 through 12 and 16-19 under 35 U.S.C. § 103 is set forth on pages 5 through 7 of the examiner's answer. On page 5 of the answer, the examiner relies upon Kasper as a teaching of using a watermark monitor to monitor the amount of data in a data queue.

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[2] Definition from Microsoft Press Computer Dictionary, Third Edition, 1997.

Dependent claims 2, 3, 9 through 12 and 16-19 all ultimately depend upon claims 1, 8 or 15, and as such contain the limitations of "pre-fetching a plurality of data from a memory to a data queue" and "delivering the data from the data queue to a bus." As addressed *supra* we do not find that Greiner teaches these limitations. We find that Kasper teaches a first in first out memory structure, which we consider to be a queue. However, we do not find that Kasper teaches or suggests that a queue should be used when pre-fetching data from memory and providing the data to a bus as is claimed. Accordingly, we will not sustain the examiner's rejection of claims 2, 3, 9 through 12 and 16-19 under 35 U.S.C. § 103.

Finally, we consider the rejection of Claims 6, 7, 13,14, 20 and 21 under 35 U.S.C. § 103 as being obvious over Greiner and official notice. The examiner's rejection of claims 6, 7, 13,14, 20 and 21 under 35 U.S.C. § 103 is set forth on pages 7 and 8 of the examiner's answer. On page 5 of the answer, the examiner takes official notice that peripheral component interconnect bus (PCI bus) is well known.

Dependent claims 6, 7, 13,14, 20 and 21 all ultimately depend upon claims 1, 8 or 15, and as such contain the limitations of "pre-fetching a plurality of data from a memory to a data queue" and "delivering the data from the data queue to a bus." As addressed *supra* we do not find that Greiner teaches these limitations. Similarly, we do not find that Greiner suggests that a queue should

be used when pre-fetching data from memory and providing the data to a bus as is claimed. Accordingly, we will not sustain the examiner's rejection of claims 6, 7, 13,14, 20 and 21 under 35 U.S.C. § 103.

In view of the forgoing, we reverse the examiner's rejection of claims 1, 4, 5, 8 and 15 under 35 U.S.C. § 102. We also reverse the examiner's rejection of claims 2, 3, 6, 7, 9 through 14, and 16 through 21 under 35 U.S.C. § 103.

REVERSED

JERRY SMITH)
Administrative Patent Judge)
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STUART S. LEVY) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
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ROBERT E. NAPPI)
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